Electronic Version
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Claims

[c1] A method of fabricating a filled trench structure, comprising:
(a) forming a first set of trenches in a first region of a substrate and forming a second set of trenches in a second region of said substrate, trenches in said first set of trenches having a higher aspect ratio than said trenches in said second region;
(b) depositing a fill material in said first and second set of trenches and on a top surface of said substrate, said fill material completely filling said trenches;
(c) removing an upper portion of said fill material; and
(d) removing, using a planarization process, all fill material from said top surface of said substrate, a top surface of said fill material in said first and second sets of trenches co-planer with said top surface of said substrate.

[c2] The method of claim 1, wherein step (c) includes wet etching, dry etching, reactive ion etching or plasma etching of said fill material.

[c3] The method of claim 1, wherein step (c) includes chemical-mechanical polishing or fixed abrasive grinding said

fill material.

[c4] The method of claim 1, further including:
between steps (b) and (c) forming a mask layer on said fill material said second region, wherein in step (c) fill material is only removed from said first region; and
between steps (c) and (d) removing said masking layer.

[c5] The method of claim 4, wherein step (c) removes about 5 to 20% of an as deposited thickness of said fill material.

[c6] The method of claim 1, wherein the aspect ratio of trenches in said first set of trenches is greater than about 3:1 and the aspect ratio of trenches in said second region is less than about 3:1.

[c7] The method of claim 1, wherein said first region is a memory cell array region and said second region is a support circuit region of an integrated circuit.

[c8] The method of claim 1, wherein said fill material is selected from the group consisting of: high-density plasma oxide, low-pressure chemical vapor deposition oxide, tetraethoxysilane oxide, silicon nitride, bis(tertiary-butylamine)silane, a thin layer of conformal insulator and a fill layer of N-doped, P-doped or undoped polysilicon, tungsten, copper or aluminum.

[c9] The method of claim 1, wherein the volume of fill material removed in step (c) is experimentally pre-determined to be a volume that allows removal in step (d) of all of said fill material from said top surface of said substrate in both said first and second regions in a predetermined amount of chemical-mechanical-polish or grind time.

[c10] The method of step 1, wherein step (c) removes about 5 to 20% of the as deposited thickness of said fill material.

[c11] A method of fabricating a filled trench structure, comprising:

(a) forming a planarization stop layer on a top surface of a substrate;

(b) forming a first set of trenches in a first region of said planarization stop layer and said substrate and forming a second set of trenches in a second region of said planarization stop layer and said substrate, trenches in said first set of trenches having a higher aspect ratio than said trenches in said second region;

(c) depositing a fill material in said first and second set of trenches and on a top surface of said planarization stop layer, said fill material completely filling said trenches;

(d) removing an upper portion of said fill material; and

(e) removing, using a planarization process, all fill material from said top surface of said planarization stop

layer, a top surface of said fill material in said first and second sets of trenches co-planer with said top surface of said planarization stop layer.

[c12] The method of claim 11, wherein step (d) includes wet etching, dry etching, reactive ion etching or plasma etching of said fill material.

[c13] The method of claim 11, wherein step (e) includes chemical-mechanical polishing or fixed abrasive grinding of said fill material.

[c14] The method of claim 11, further including:
between steps (c) and (d) forming a mask layer on said fill material in said second region, wherein in step (d) fill material is only removed from said first region; and
between steps (d) and (e) removing said masking layer.

[c15] The method of claim 14, wherein step (d) removes about 5 to 20% of an as deposited thickness of said fill material.

[c16] The method of claim 11, wherein the aspect ratio of trenches in said first set of trenches is greater than about 3:1 and the aspect ratio of trenches in said second region is less than about 3:1.

[c17] The method of claim 11, wherein said first region is a

memory cell array region and said second region is a support circuit region of an integrated circuit.

[c18] The method of claim 11, wherein said fill material is selected from the group consisting of: high-density plasma oxide, low-pressure chemical vapor deposition oxide, tetraethoxysilane oxide, silicon nitride, bis(tertiary-butylamine)silane, a thin layer of conformal insulator and a fill layer of N-doped, P-doped or undoped polysilicon, tungsten, copper or aluminum.

[c19] The method of claim 11, wherein the volume of fill material removed in step (d) is experimentally predetermined to be a volume that allows removal in step (e) of all of said fill material from said top surface of said substrate in both said first and second regions in a predetermined amount of chemical-mechanical-polish or grind time.

[c20] The method of step 11, wherein step (d) removes about 5 to 20% of the as deposited thickness of said fill material.